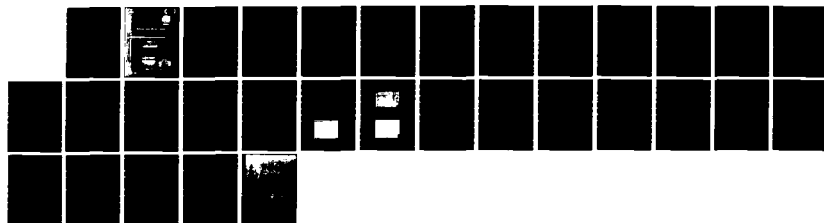AD-A132 373 THE BJT-JFET A NOVEL MERGED DEVICE STRUCTURE(U) HAWAII   1/1
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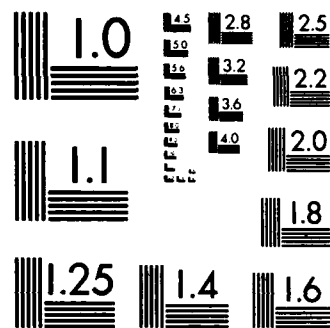   L TAN ET AL. JUL 83 N00014-76-C-1081

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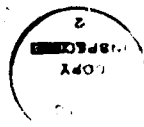1 JAN 73

THE BJT-JFET*, A NOVEL MERGED DEVICE STRUCTURE

by

Leng-Seow Tan

and

James W. Holm-Kennedy,
Principal Investigator

*The BJT-JFET was proposed by Prof. James W. Holm-Kennedy, Electrical Engineering Department, University of Hawaii.

Patent pending. Work supported in part by the University of Hawaii.

ABSTRACT

A novel semiconductor device, the BJT-JFET, is described. The
fabrication of the device is described and the device characteristics
are explained in terms of the fully merged nature of the device and the
self-biasing effects of the distributed collector current on the collector/
channel base bias. A simple analytical model is developed. The results
are consistent with the conceptual understanding of the operation
of the device.

INTRODUCTION

A novel solid state device* is described in this report. Development work on the device is currently being continued by Lengseow Tan, a graduate student, and Professor James Holm-Kennedy. The report is divided into three major sections. In the first section the structure and operation of the device is explained from a conceptual point of view. The second section of the report describes the experimental work which has been carried out. In the third section a simple, first order analytical model of the device is presented.

SECTION (1): PRINCIPLE OF OPERATION OF THE BJT-JFET

1.1 Structure of the Device

A schematic diagram of the device structure is shown in Fig. 1.1. The device consists of four layers of alternately p-type and n-type silicon. The lower three layers form an n-p-n bipolar junction transistor (BJT). The n-type collector layer also serves as the channel of a junction field effect transistor (JFET), with the adjacent p-type regions acting as the gates of the JFET. An n^+ region at one end of the collector/channel provides ohmic contact to the collector/drain terminal.† The device is therefore a fully merged and distributed BJT-JFET and its operation contains features of both the BJT and the JFET as well as other novel features with useful applications of particular interest.

1.2 Basic Principle of Operation

The basic principle of operation of the BJT-JFET is illustrated in Fig. 1.2. The device is operated here with the BJT biased in the forward active mode. The emitter is grounded and the emitter-base junction is forward-biased. Holes are injected from the base into the emitter. Because of the injection efficiency of the BJT, for every hole injected from the base into the emitter, a large number of electrons are injected from the emitter into the base. Most of the electrons diffuse across the thin base region to arrive at the base-collector junction, which is reverse-biased. The electric field at the base-collector junction sweeps the electrons into the collector/channel. The electrons drift along the collector/channel and are finally collected at the collector/drain contact to constitute the FET drain current I_C and BJT collector current. A small base current I_B provides the holes for recombination in the base and for injection into the emitter.

The drain current I_C of the BJT-JFET can be controlled by varying the base current I_B of the BJT portion of the device, or by varying the gate voltage V_{GE} of the JFET. Increasing I_B tends to increase the collector current of the BJT, as is evident from the operation of a conventional bipolar transistor. On the other hand, increasing the reverse bias on the gate (i.e., making V_{GE} more negative) will reduce the channel cross-section and tends to reduce the channel/collector current. Thus, the drain current I_C is a function of the drain voltage V_{DE} as well as the gate voltage V_{GE} and the base current I_B in this novel four terminal device.

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*Proposed by Prof. James W. Holm-Kennedy, Electrical Engineering Department, University of Hawaii. The device is similar in certain respects to the MOSBJT described in ONR Reports I and II by Okada and Holm-Kennedy.

†The channel can also be used as the emitter instead of the collector of the BJT, in another mode of operation of the device.
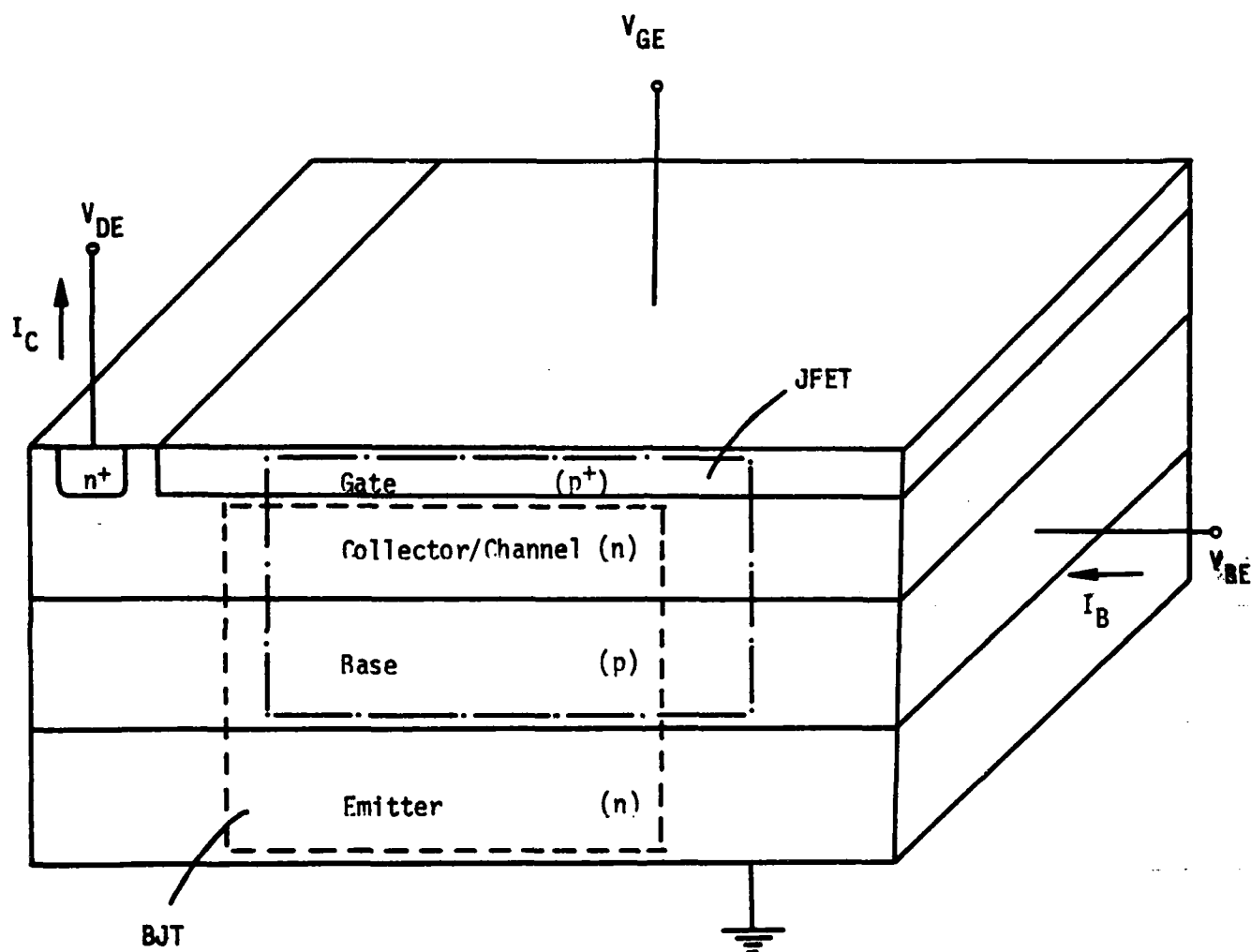
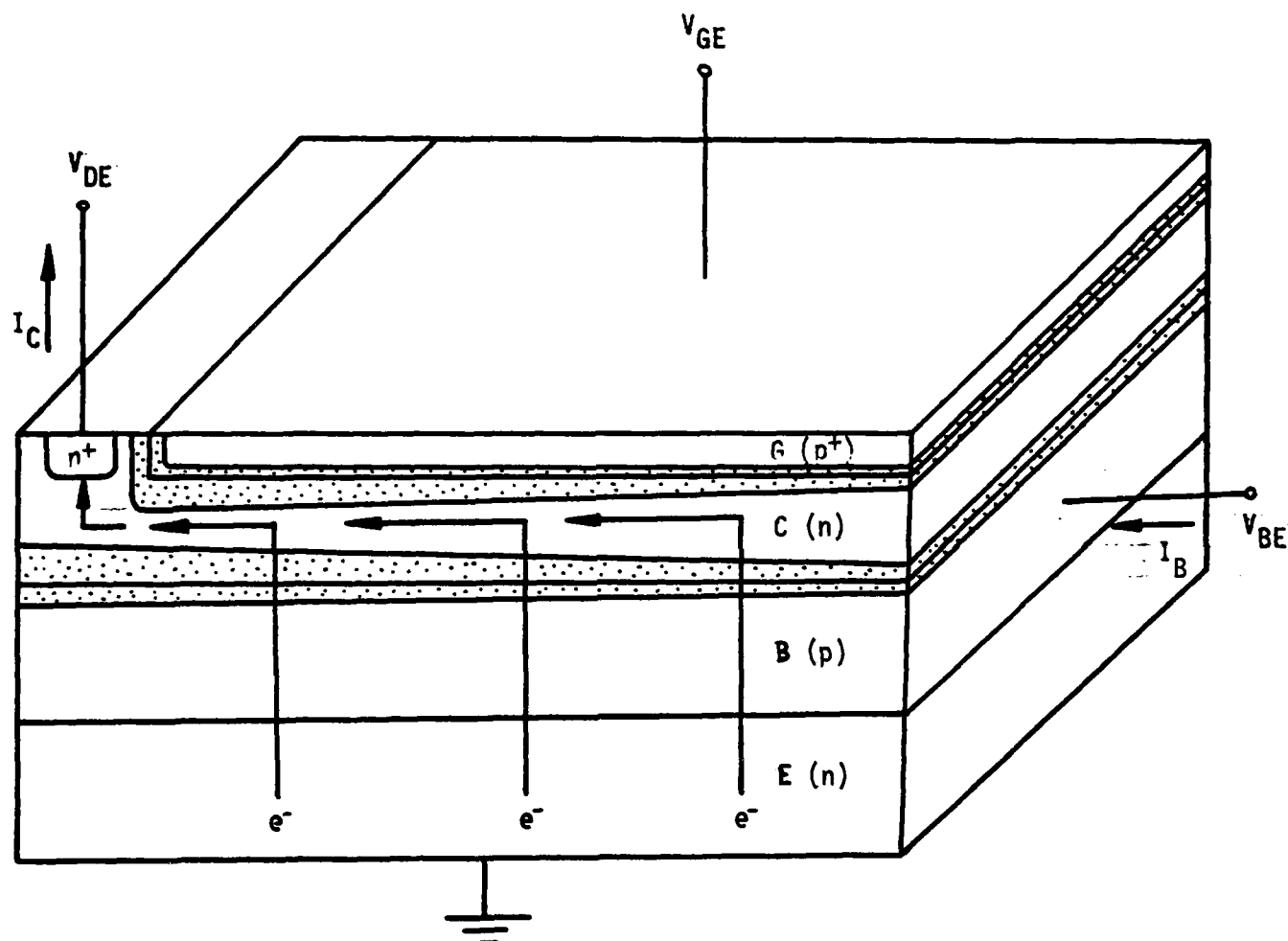Fig. 1.1 : Structure of the BJT-JFET.

Fig. 1.2 : Diagram showing basic operation of the BJT-JFET.

1.3 Non-linearity in the BJT-JFET

An interesting and unusual behavior of the BJT-JFET occurs when the device is operated under appropriate bias. Figure 1.3(a) shows a cross-section of the device. Figures 1.3(b), 1.3(c) and 1.3(d) show the energy band diagrams corresponding to the different regions of operation.

To help in clarifying the operation of the device, the following voltages are assumed:

$\quad$ (i) Emitter voltage V_E = 0 V as the emitter is grounded

$\quad$ (ii) Base voltage V_B = 0.7V as the emitter-base junction is forward biased.

$\quad$ (iii) Drain voltage V_{DE} = 10V.

The voltage along the channel/collector is not constant but decreases progressively away from the drain contact X_D because of the resistive voltage drop along the channel. Thus, at point X_D in Fig. 1.3(a) the channel voltage $V_C(D)$ = drain voltage V_{DE} = 10V. The voltage at a point X_F, further back, will be lower, say 5V for instance. As long as the channel voltage is greater than 0.7V, so that the base-collector bias V_{BC} is negative, the collector/channel will collect the electrons which have diffused across the base to the edge of the base-collector junction. The bipolar transistor will operate in the forward-active mode, as shown by the energy band diagram in Fig. 1.3(b). Point X_A at which the channel voltage $V_C(X_A)$ = 0.7V defines the limit of the 'on' region of the BJT. (The 'on' region is the forward active bias region.)

At point X_T the channel voltage $V_C(X_T)$ is less than 0.7V. For instance, if $V_C(X_T)$ = 0.5V, then $V_{BC} = V_B - V_C(X_T) = 0.7 - 0.5 = 0.2V$. The base-collector junction is thus here forward-biased and this portion of the BJT is operating in the saturation mode. That is, part of the BJT is operating in the forward active mode while simultaneously the rest of the device is operating in saturation, a nonordinary situation with particular device applications. The electron distribution profile in the base is shown in Fig. 1.3(c), superimposed on the energy band diagram. As can be seen in Fig. 1.3(c), the gradient of the electron distribution profile is much less than the corresponding profile in Fig. 1.3(b), where the BJT is in the active mode. The electron flux crossing the base and hence the channel current, is much smaller in the 'transition' region than in the 'on' region of the device.

At point X_O, the channel voltage $V_C(X_O)$ is even lower than that at X_T, say 0.3V, for example. The base-collector junction at X_O is more forward-biased than at X_T, so that the injection from the collector into the base is greater. The base electron distribution profile is flat, as shown in Fig. 1.3(d). Because of the flat profile, electrons which have been injected from the emitter and the collector into the base remain in the base until they recombine with holes supplied by the base current. The portion of the BJT in the 'off' region therefore does not contribute any current to the collector/channel.

There are therefore three regions of operation in the BJT-JFET: an 'on' region, an 'off' region and a transition region in between.* The limit of the

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*Holm-Kennedy and Okada first proposed the modulation effect on the active area of this class of devices and its effects on device nonlinearities. See ONR Final Reports I and II.
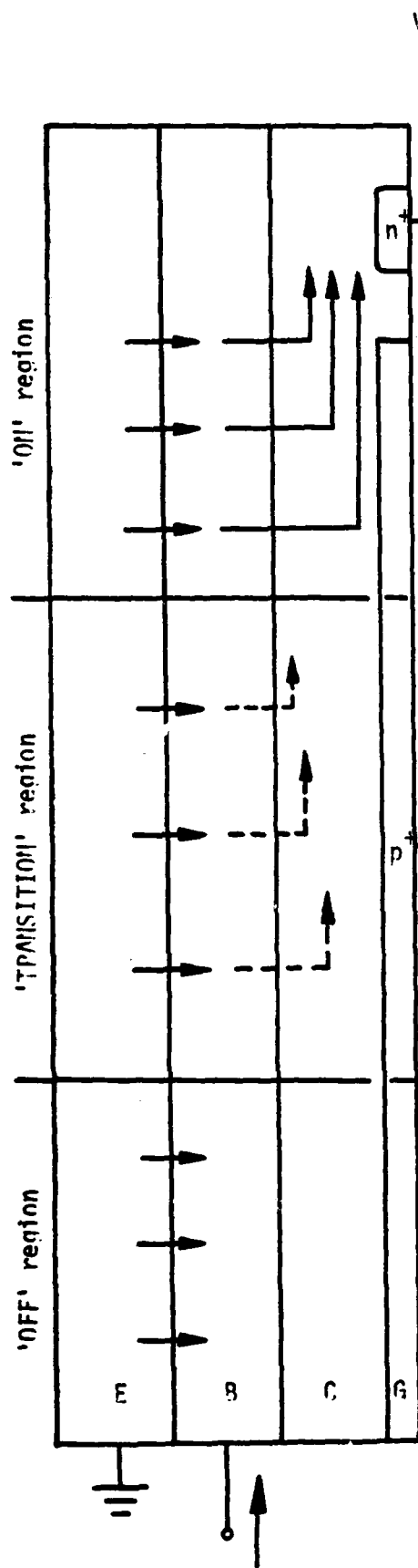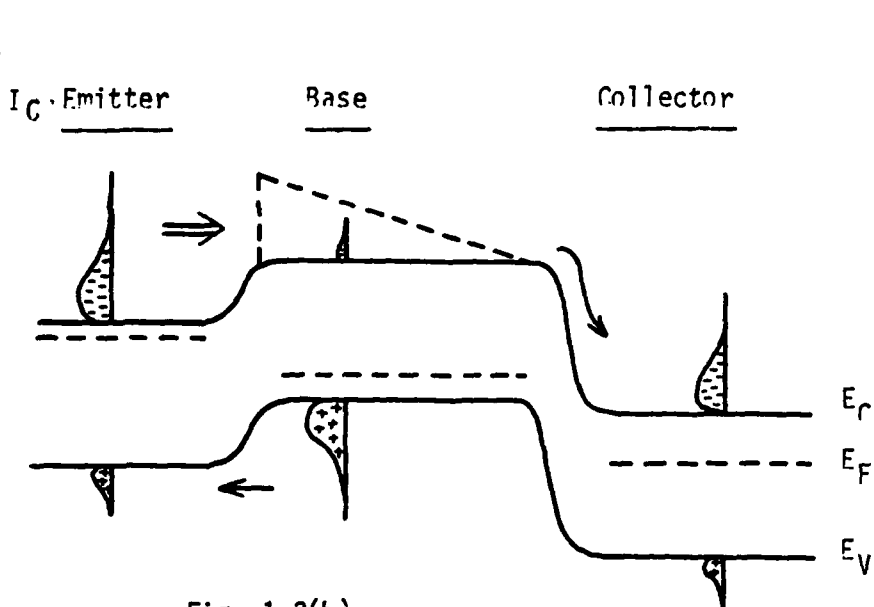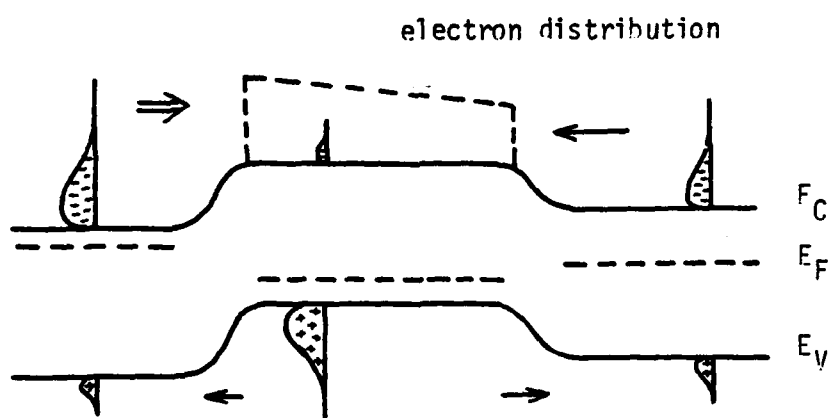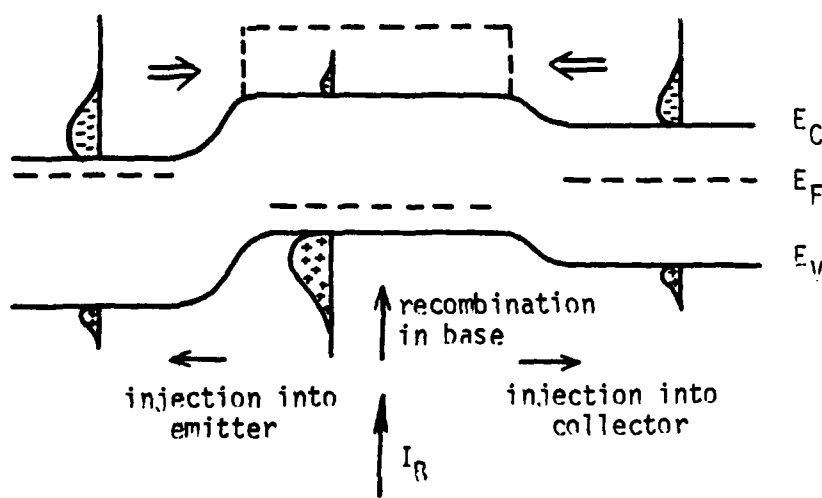
Fig. 1.3(a)

Fig. 1.3(b)

Fig. 1.3(c)

Fig. 1.3(d)

electron distribution

recombination
in base

injection into
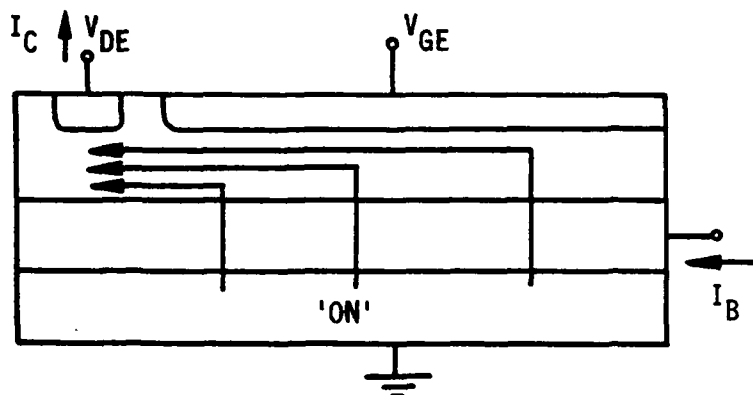emitter

injection into
collector

-6-

Fig. 1.4(a) : Low I_B or $|V_{GE}|$, entire device 'ON'.
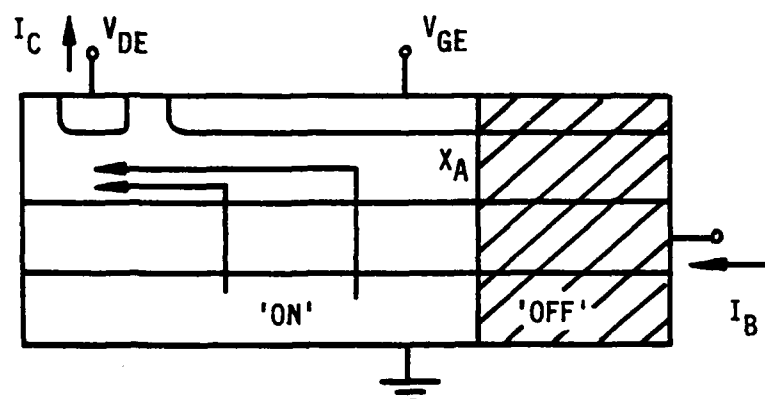
Fig. 1.4(b) : Moderate I_B or $|V_{GE}|$, a small portion of the device is 'OFF'.
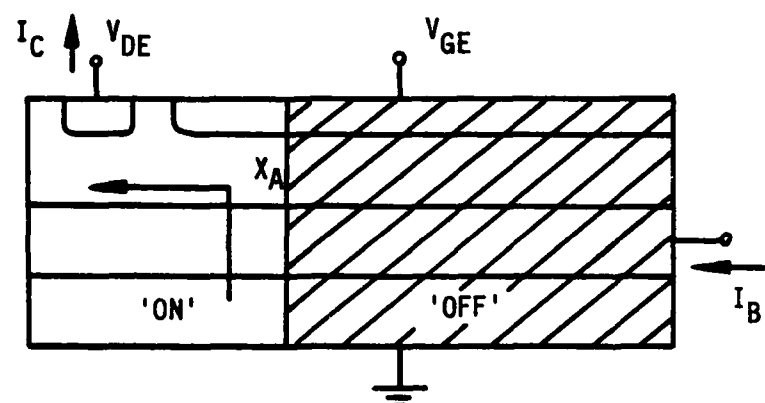
Fig. 1.4(c) : High I_B or $|V_{GE}|$, a large portion of the device is 'OFF'.

Note : The transition regions between the 'ON' and 'OFF' regions have been omitted for the sake of clarity.

'on' region is the point X_A where the channel voltage is so low (0.7V) that the base-collector junction is no longer biased to collect the injected electrons. The position of the point X_A in the channel in turn depends on the voltage drop along the channel. If the voltage drop along the channel is large, the point X_A will be nearer the drain end of the channel, and vice versa.

The voltage drop along the channel is a function of the channel current and the channel resistance. When the base current is low, the collector/channel current is also low so that the voltage drop along the channel is small. It may then be that there is nowhere in the channel where the voltage is lower than 0.7V, and the entire channel/collector is collecting electrons from the base. This situation is depicted in Fig. 1.4(a). When the base current is increased, the channel/collector current will also increase (bipolar transistor action). The higher channel/collector current will cause a higher voltage drop along the channel. At the point X_A, Fig. 1.4(b), the channel voltage has decreased to 0.7V. Beyond this point, the channel/collector is no longer reverse-biased with respect to the base and is thus not collecting electrons from the base. The portion of the device to the right of the point X_A in Fig. 1.4(b) is therefore 'off'. If the base current is further increased, the voltage drop along the channel/collect will be more rapid and the point X_A will move closer to the drain, as shown in Fig. 1.4(c). A larger proportion of the device will be 'off'.

The variation of the volumes of the 'on' and 'off' regions of the BJT-JFET introduces an element of non-linearity in the device. Suppose the base current is increased by 20%. In a conventional BJT, this would increase the collector current by 20% if the BJT is biased to operate as a linear amplifier. In the BJT-JFET, however, increasing the base current also tends to reduce the volume of the 'on' portion of the device. Because of this reduction of the 'on' volume of the device, a 20% increase in the base current may result only in a 5% increase in the channel/collector current, thus producing a nonlinear dependence of the channel/collector current on the base current. This nonlinearity in the operation of the BJT-JFET is useful in applications such as harmonic generation and the mixing of two signals. Sources of nonlinearity due to conventional pinch off effects in the channel can occur and these too can lead to useful applications.

SECTION (2): EXPERIMENTAL WORK

2.1 Fabrication of the BJT-JFET

The BJT-JFET which was described in Section (1) was fabricated in the Physical Electronics Laboratory of the University of Hawaii. The major steps in the fabrication procedure are summarized below and in Figs. (2.1)-(2.6).

(a) Starting with an n-type silicon wafer, a wet oxide is grown at 1100°C, 45 min.

(b) Using standard photoresist procedure, windows are opened in the oxide for a boron diffusion to form the base of the BJT. The boron predeposition diffusion is carried out at 800°C for 20 min. and the drive-in diffusion at 1100°C for 40 min. During the drive-in diffusion, a wet oxide is grown to block the out-diffusion of the boron atoms. This oxide layer is also used as the masking oxide for the subsequent phosphorus diffusion.

-8-

(c) Windows are opened in the oxide layer (using standard photoresist procedure) for a phosphorus diffusion to form the emitter of the BJT. The phosphorus predeposition diffusion is carried out at 800°C for 30 min and the drive-in diffusion at 950°C for 20 min. As in step (b), a wet oxide is grown during the drive-in diffusion to block the out-diffusion of phosphorus and to serve as the blocking oxide for the next diffusion.

(d) Standard photoresist procedure is used to open windows in the oxide layer for a boron diffusion to form the gate of the JFET. The boron predeposition diffusion is carried out at 900°C for 20 min.

(e) A wet oxide is grown over the wafer as the masking oxide for the next diffusion. The oxide growth is carried out at 900°C for 60 min.

(f) Windows are opened in the oxide layer by standard photoresist pro-cedure. A phosphorus predeposition diffusion is then carried out at 900°C for 30 min to form n^+ regions in the n-type emitter and collector of the BJT. These n^+ regions will allow ohmic contacts to be formed with n-type regions when aluminum is deposited on the device.

(g) A wet oxide is grown over the wafer at 900°C for 60 min. Windows are etched in the oxide to allow contacts to be made to the col-lector, base, emitter and gate of the device.

(h) Aluminum is deposited over the wafer using the vacuum deposition technique.

(i) Metal contacts are defined on the wafer using standard photoresist procedure. Excess aluminum on the wafer is etched off. Finally the wafer is sintered at 450°C for 3 min. followed by a solid phase regrowth process to ensure good ohmic contact between the aluminum and the p and n^+ regions of the finished device.

A cross-sectional view of the BJT-JFET fabricated by the above procedure is shown in Fig. 2.6. This device is slightly different from that shown in Fig. 1.1 of Section (1) as the substrate is used as the collector instead of the emitter of the BJT. For a BJT to operate with sufficient gain, the injection efficiency at the emitter-base junction must be high, which in turn requires that the emitter be more heavily doped than the base. In the fabrication procedure described above, the BJT-JFET is made by a series of diffusions on an n-type substrate. The n-substrate must therefore be more lightly-doped than the p-type (base) region above it since the p-type region is formed by diffusing in p-type dopants to over-compensate the n-type dopants originally present in the substrate. If the BJT so fabricated is operated with the substrate as the emitter, the injection effi-ciency of the BJT would be very low. Thus, to obtain sufficient gain for the device, the BJT-JFET is operated with the substrate as the collector and the diffused n-region above the base as the emitter. Other fabrication procedures would allow the JFET to be placed at the top.
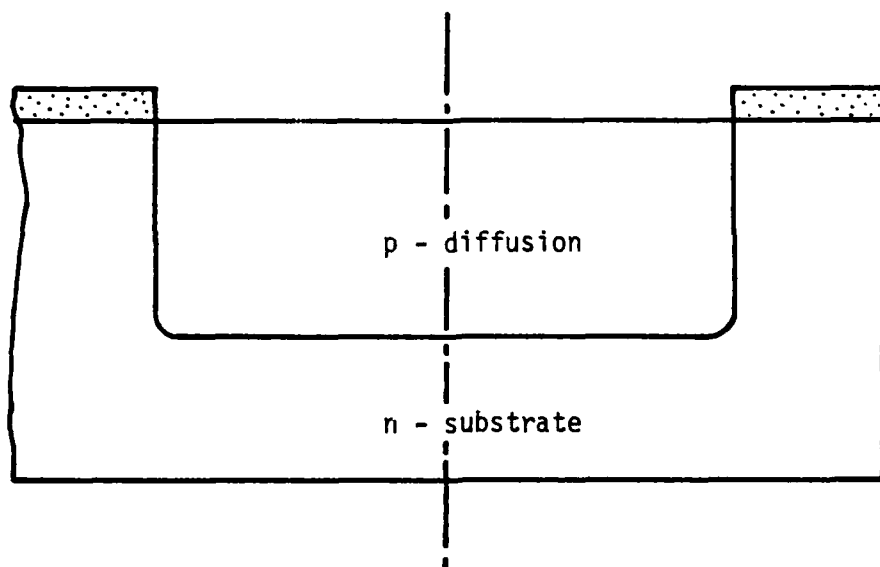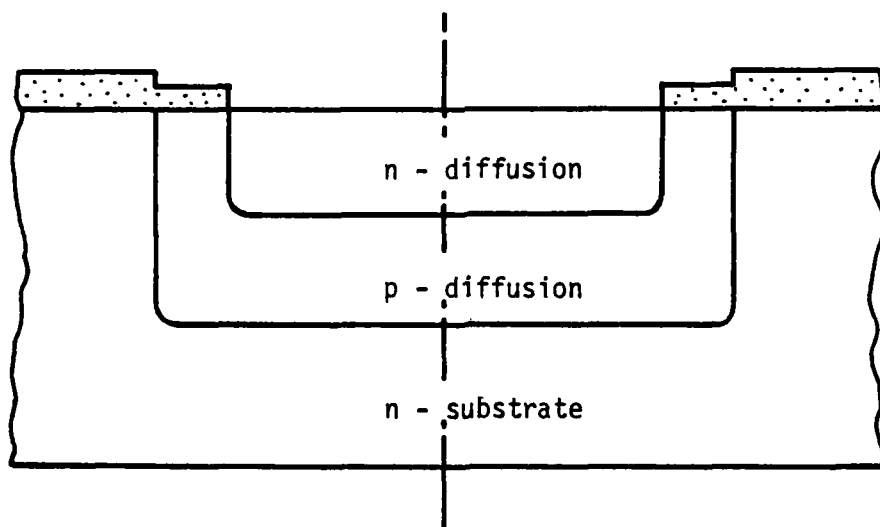
Fig. 2.1 : Base diffusion.

Fig. 2.2 : Emitter diffusion.
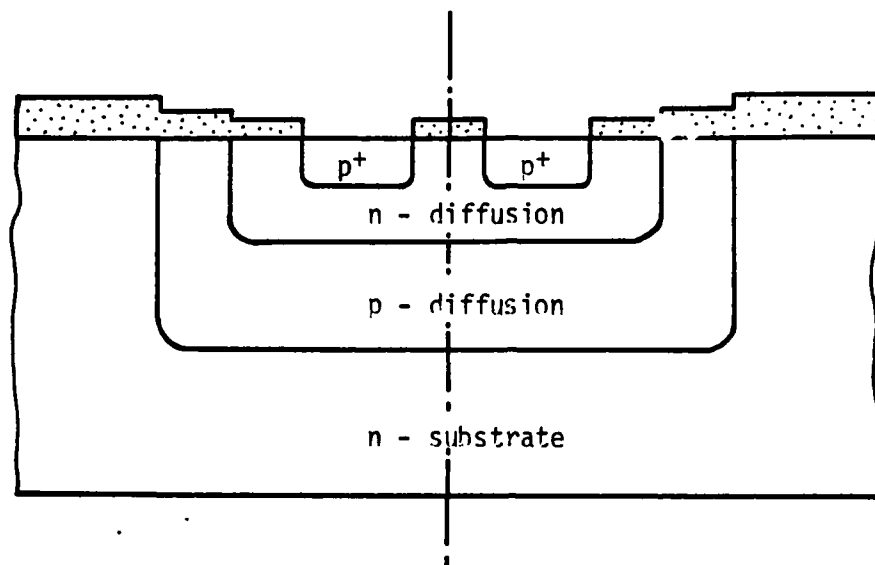
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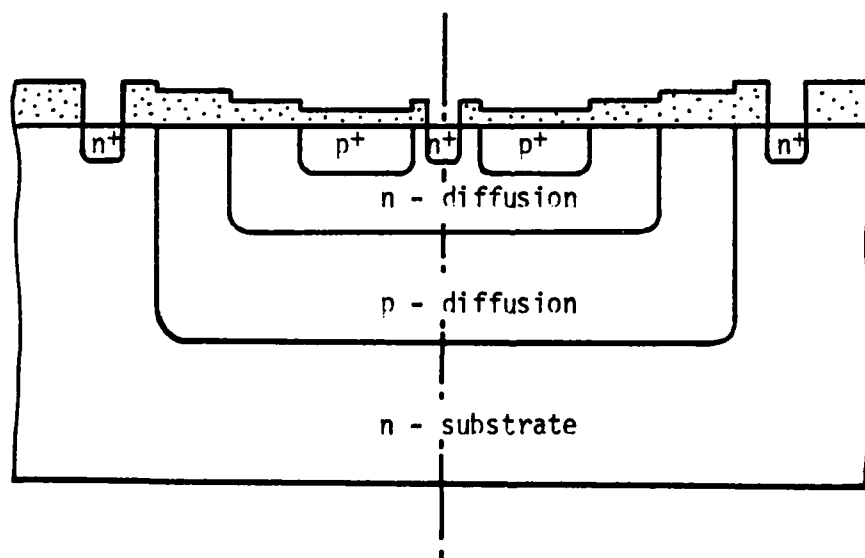Fig. 2.3 : Gate diffusion.

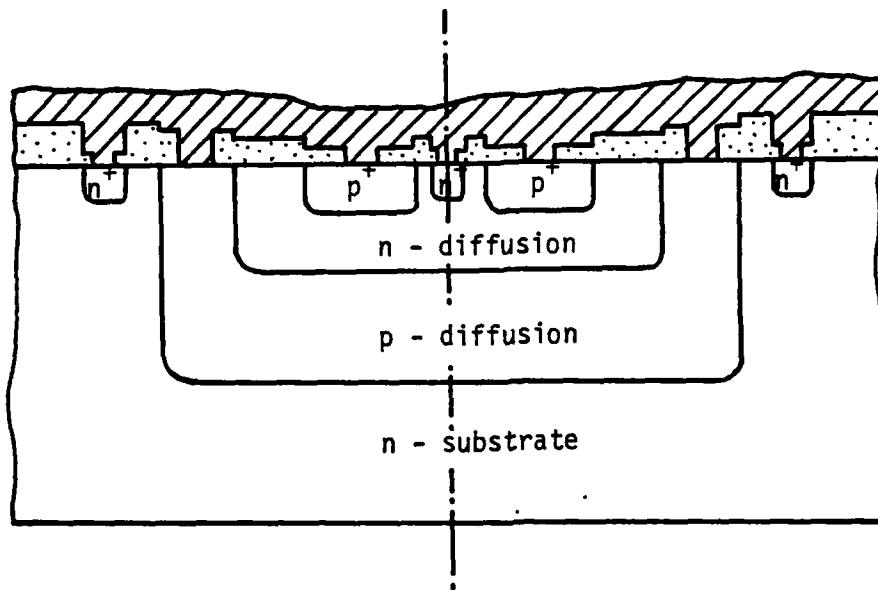Fig. 2.4 : n$^+$ diffusion for ohmic contacts to n-type regions.

Fig. 2.5 : Metalization.

Fig. 2.6 : Finished device.

░░░	Silicon dioxide
▨▨▨	Aluminium

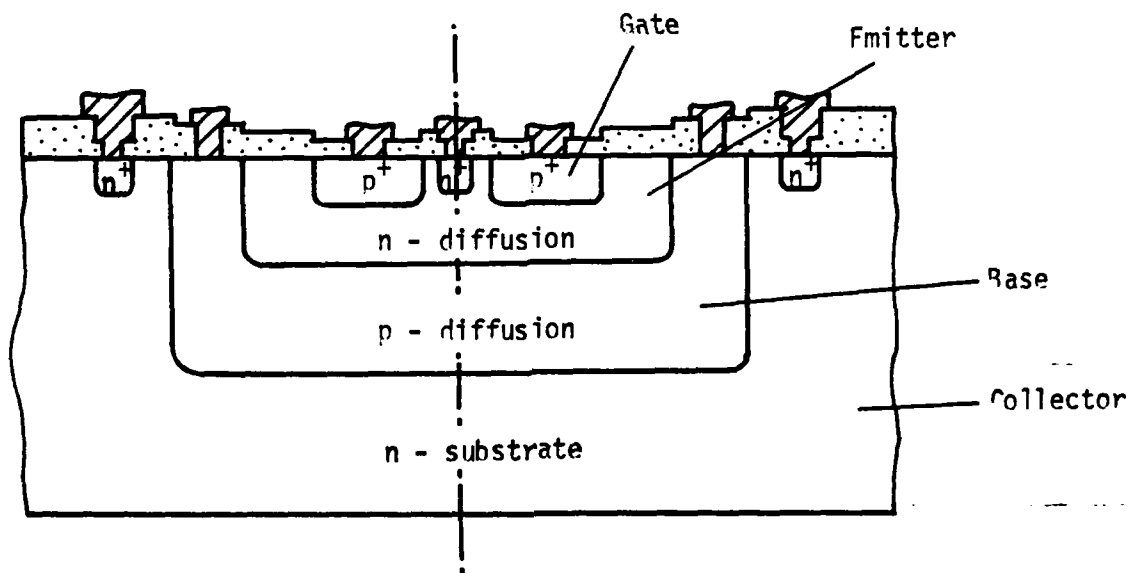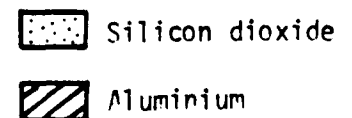## 2.2 Problems Encountered in the Fabrication of the BJT-JFET

The dopant concentration profile of the BJT-JFET fabricated by the procedure described above is shown in Fig. 2.7. The profile is calculated with the aid of a computer program developed at the U.H. Physical Electronics Laboratory* and implemented on a HP 9836 microcomputer. Figure 2.7 shows the substrate dopant concentration as well as the dopant concentrations of the three diffusions carried out to form the base, emitter and gate of the BJT-JFET. Because each diffused layer is formed by over-compensation of the previous diffusion, the dopant concentrations must become progressively higher for succeeding diffusions. Thus, the base is more highly doped than the collector, the emitter is more highly doped than the base, and so on. Near the surface of the wafer, the dopant concentrations of the p-type gate region and the n-type emitter/channel region may be so high that a tunnelling junction may develop between the gate and the emitter/ channel. This situation can only be prevented by careful control of the diffusion time and diffusion temperature to ensure that the dopant concentrations are not sufficiently high for tunnelling to occur.

There is another problem associated with the triple diffusion process that is used to fabricate the BJT-JFET. Consider, as an example, the position of the junction between the n-type substrate (collector) and the p-type base diffusion. The junction depth is determined primarily by the temperature and duration of the base drive-in diffusion. However, during subsequent high temperature processes (diffusion and oxidation) to form the emitter and gate of the device, the boron dopant atoms in the base will diffuse further into the substrate, thus making the base-collector junction deeper than intended.

The above problem is overcome by using an effective diffusivity D_{eff} for the dopant atoms[†] (e.g. boron, for the base diffusion) when calculating the time duration required for the drive-in process, using the equation

$$D_{eff} = \frac{D_1 t_1 + D_2 t_2 + D_3 t_3 + \ldots}{t_1 + t_2 + t_3} \qquad (2.1)$$

where D_1 is the diffusivity of the dopant (boron) atoms at the temperature of the drive-in process, t_1 is the time duration of the drive-in, $t_2, t_3, \ldots$ and $D_2, D_3, \ldots$ are the respective time duration and diffusivities of the boron atoms in subsequent high temperature processes.

2.3 Experimental Results

Three sets of the I-V characteristics of the BJT-JFET are shown in Figs. 2.9, 2.10, 2.11. These characteristics are taken directly from a transistor curve tracer and show the collector/channel current I_C versus the collector/drain voltage V_{CE}/V_{DE} for various base current I_B. The gate bias V_G is 0V in Fig. 2.9, -1V in Fig. 2.10 and -2V in Fig. 2.11. The biasing arrangement to produce the I-V characteristics is shown in Fig. 2.8.

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*The computer program was developed by Daniel R. Morgan.

[†]D.J. Hamilton and W.G. Howard, Basic Integrated Circuit Engineering, p. 47, McGraw-Hill, New York (1975).
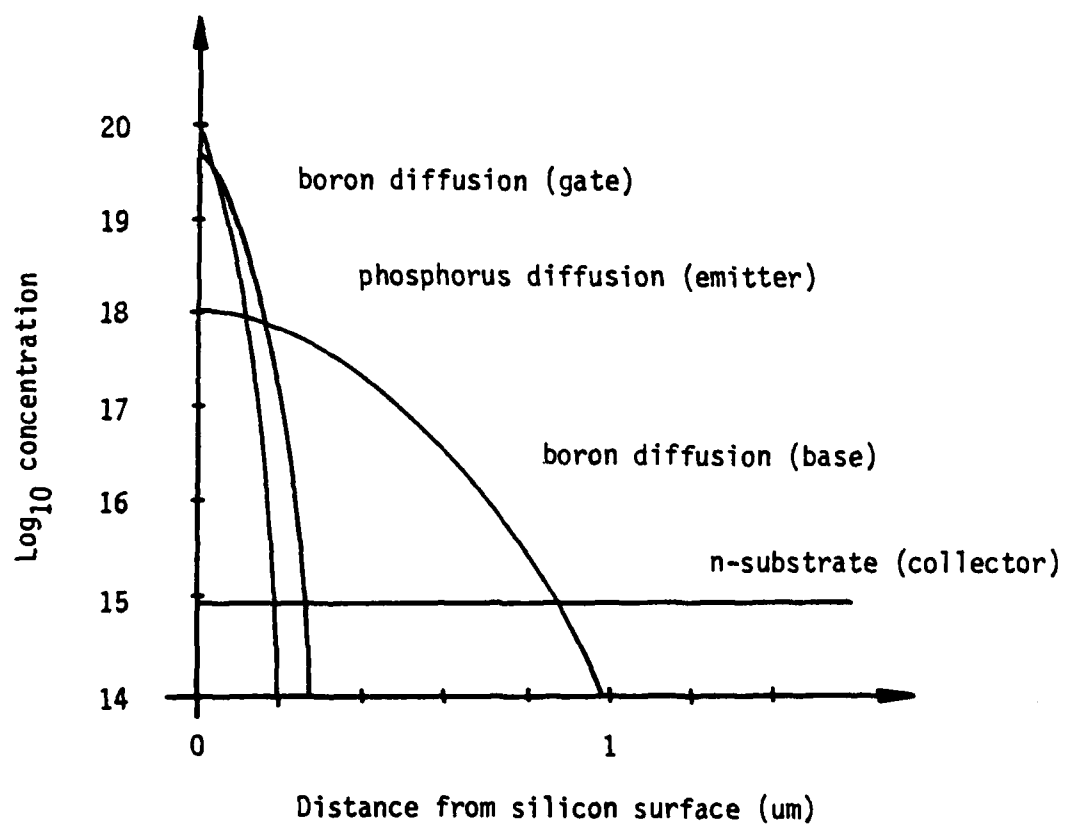
Fig. 2.7 : Dopant concentration profile for the triple diffused BJT-JFET.

Fig. 2.8 : Biasing arrangements for obtaining the I - V characteristics
of the BJT-JFET characteristics in Figs. 2.9, 2.10, 2.11.

Fig. 2.9 : BJT-JFET characteristics. I_C versus V_{CE} for
various I_B. V_G=0 volt.

Fig. 2.10 : BJT-JFET characteristics. I_C versus V_{CE} for various I_B. V_G=-1 volt.

Fig. 2.11 : BJT-JFET characteristics. I_C versus V_{CE} for various I_B. V_G=-2 volts.

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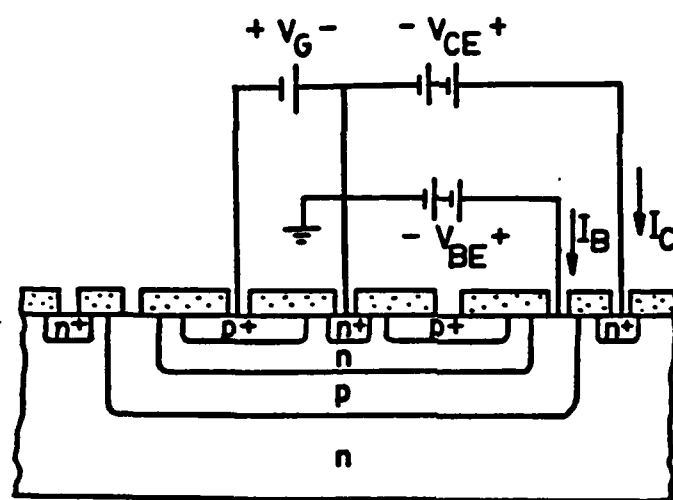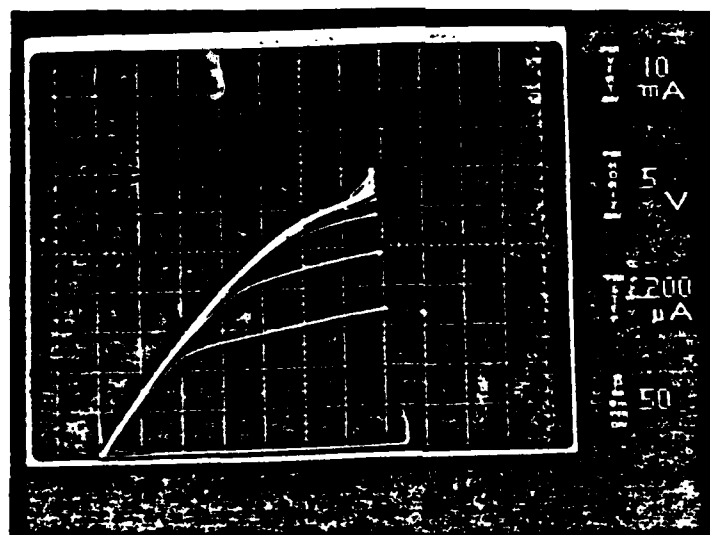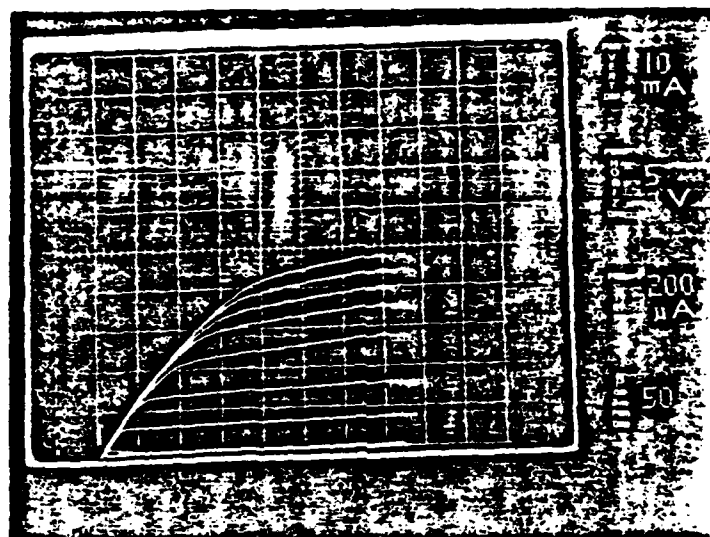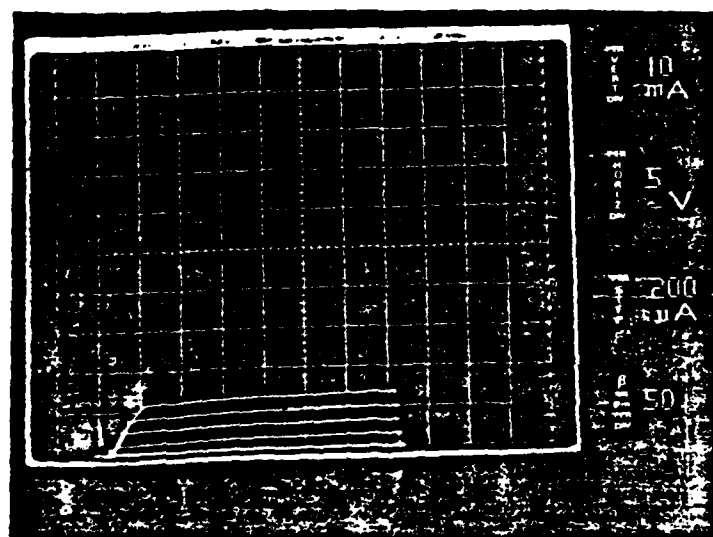The characteristics in Fig. 2.9 show the nonlinear dependence of the collector/channel current I_C on the base current I_B, which is consistent with principle of operation of the BJT-JFET described in Section (1) of this report. Initially, I_C increases rapidly with increasing I_B. The increase in I_C becomes less and less, however, and I_C finally saturates around 60 mA. Physically this behavior of I_C can be explained by an increasingly larger portion of the device turning 'off' with increasing I_B (see Fig. 1.4(a) - 1.4(c), Section (1)). Finally, under high bias, only the small portion of the device directly under the n^+ diffusion (Fig. 2.8) is 'on'. (The β shown in the figures is modest but is easily increased by using a different fabrication procedure. The goal here is to demonstrate the essential characters of the device, not to achieve a large β.

When a reverse bias is applied to the gate, the depletion region adjacent to the channel widens, thus narrowing the conducting channel. The channel resistance increases which in turn tends to reduce the collector current. This effect is shown in Fig. 2.10 and Fig. 2.11 where it is noted that the collector current decreases for progressively higher reverse gate bias.

The experimental results show that the BJT-JFET is a nonlinear amplifying or switching device in which the transistor characteristics (I_C versus V_{CE} for different I_B's) can be modified by the application of a bias on the gate terminal.

SECTION (3): ANALYTICAL MODEL

A first order analytical model of the BJT-JFET is presented in this section.* A diagram of the device and the symbols used in the analysis are shown in Fig. 3.1.

Several assumptions were made to simplify the analysis:

    (a) In the region where the BJT is 'on', the current density J_C injected into the channel/collector (by transistor action of the BJT) is uniform, i.e., J_C is not a function of x or y. In the 'off' region of the BJT, $J_C=0$. The transition between the 'on' and 'off' regions of the BJT is assumed to occur abruptly at the point where the channel voltage $V_C(y)=0$.

    (b) Channel doping is uniform, i.e., the resistivity ρ of the channel is not a function of x or y.

    (c) The gradual channel approximation is assumed. This approximation states that the channel and depletion layer widths vary slowly from source to drain so that the depletion region is influenced only by fields in the x-direction. This assumption allows modelling of the BJT-JFET using a one-dimensional analysis which not only simplifies the problem but provides useful insights into the operation of the device. A two-dimensional analysis of the problem may be more accurate but would also be less tractable mathematically and would require extensive computer-aided analysis.

With reference to Fig. 3.1, consider an element of the channel of length dy, distance y from the drain end (y=0) of the channel. The incremental resistance dR(y) of this element is given by

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*The approach adopted in this section parallels the approach originally used by Okada to analyze the MOSBJT.

L

V_{DE}

W

I_C

V_{GE}

x_{d1}

n^+

t

$x_c(y)$

V_{BE}

x_{d2}

I_B

J_C

y

dy

BJT 'ON' region

BJT 'OFF' region

$y = 0$

$y = \ell$

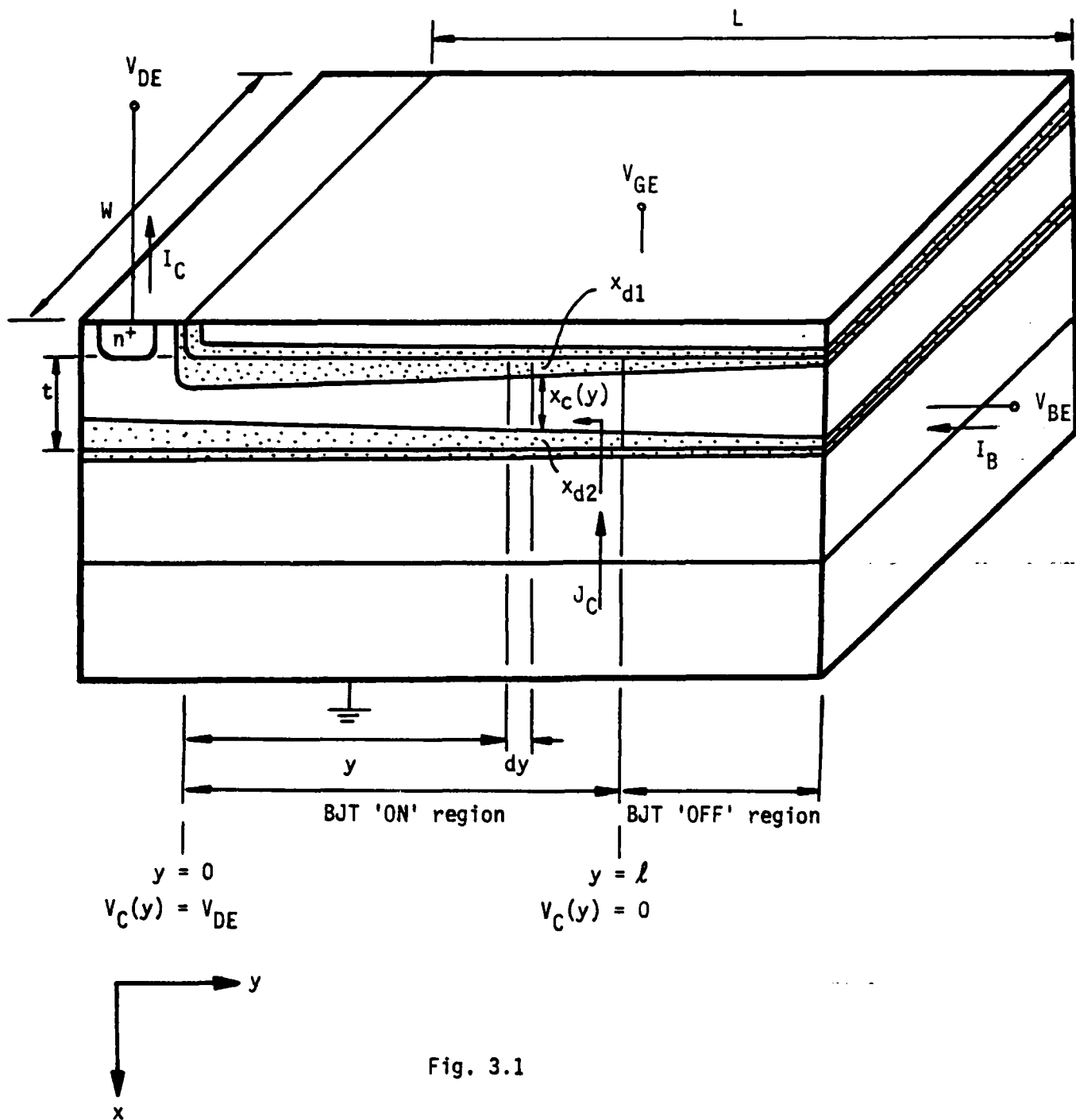$V_C(y) = V_{DE}$

$V_C(y) = 0$

y

x

Fig. 3.1

Note : The direction of J_C in the figure above is the direction of the
electron flux, which is opposite to the direction of positive current.

$$dR(y) = \frac{\rho dy}{W x_C(y)} \qquad (3.1)$$

where ρ is the resistivity of the channel,
W is the lateral dimension of the channel, and
$x_C(y)$ is the width of the channel.

The current flowing through this element of the channel is equal to all the current that is injected into that part of the channel/collector from y to ℓ, (see Fig. 3.1), i.e.,

$$I(y) = J_C W(\ell-y) \qquad (3.2)$$

where J_C is the current density of the injection (by transistor action of the BJT) into the channel/collector.

The incremental channel voltage drop across the element dy is

$$dV_C(y) = -I(y)dR(y) . \qquad (3.3)$$

The negative sign in Eq. (3.3) arises because the channel voltage $V_C(y)$ decreases in the direction of increasing y.

By substituting for $I(y)$ and $dR(y)$ in Eq. (3.3), we get

$$dV_C(y) = -\rho J_C \frac{(\ell-y)}{x_C(y)} dy \qquad (3.4)$$

$x_C(y)$ can be be expressed as

$$x_C(y) = t - x_{d1} - x_{d2} \qquad (3.5)$$

where t is the width of the channel/collector, inclusive of the depletion layers, x_{d1} is the width of the depletion layer at the gate/channel junction, x_{d2} is the width of the depletion layer at the base/channel junction.

From p-n junction theory,

$$x_{d1} = [\frac{2\epsilon_s}{qN_d} (V_{bi} + V_C(y) - V_{GE})]^{\frac{1}{2}} , \qquad (3.6)$$

and

$$x_{d2} = [\frac{2\epsilon_s}{qN_d} (V_{bi} + V_C(y) - V_{BE}]^{\frac{1}{2}} , \qquad (3.7)$$

where V_{bi} is the built-in potential across an unbiased p-n junction,
V_{GE} is the applied gate voltage,
V_{BE} is the applied base voltage,
$V_C(y)$ is the channel voltage,
ϵ_s is the permittivity of silicon,
q is the electronic charge and
N_d is the dopant concentration in the channel/collector.

Substituting for $x_C(y)$ in Eq. (3.4) and rearranging terms, we have

$$-pJ_C(\ell-y)dy = \left\{ t - \left[\frac{2\varepsilon_s}{qN_d}(V_{bi} + V_C(y) - V_{GE})\right]^{\frac{1}{2}} - \left[\frac{2\varepsilon_s}{qN_d}(V_{bi} + V_C(y) - V_{BE})\right]^{\frac{1}{2}}\right\}dV_C(y) \tag{3.8}$$

The total voltage drop along the channel is the sum of all the incremental voltage drops $V_C(y)$ from $y=\ell$ to $y=0$. The boundary conditions are:

$$\text{at } y = 0, \qquad V_C(y) = V_{DE} ; \tag{3.9}$$

$$\text{at } y = \ell, \qquad V_C(y) = 0 . \tag{3.10}$$

Integrating both sides of Eq. (3.8),

$$-pJ_C\int_0^{\ell}(\ell-y)dy = -\int_0^{V_{DE}}\left\{ t - \left[\frac{2\varepsilon_s}{qN_d}(V_{bi} + V_C(y) - V_{GE})\right]^{\frac{1}{2}} - \left[\frac{2\varepsilon_s}{qN_d}(V_{bi} + V_C(y) - V_{BE})\right]^{\frac{1}{2}}\right\}dV_C(y) \tag{3.11}$$

that is,

$$\ell^2 = \frac{1}{J_C}\frac{2}{\rho}\left\{ V_{DE}t - \frac{2}{3}\left(\frac{2\varepsilon_s}{qN_d}\right)^{\frac{1}{2}}\left[(V_{bi} - V_{GE} + V_{DE})^{3/2} - (V_{bi} - V_{GE})^{3/2}\right] - \frac{2}{3}\left(\frac{2\varepsilon_s}{qN_d}\right)^{\frac{1}{2}}\left[(V_{bi} - V_{BE} + V_{DE})^{3/2} - (V_{bi} - V_{BE})^{3/2}\right]\right\} \tag{3.12}$$

The collector current density J_C in Eq. (3.12) can be expressed in terms of the base current density J_B, which consists of several components (Fig. 3.2(a)):

(a) In the 'on' region of the BJT-JFET, the BJT is biased in the forward active mode. The base current supplies holes for recombination in the base and injection into the emitter. If the current gain of the BJT in the 'on' region is denoted by β_{ON}, then

$$J_{B,ON} = \frac{J_C}{\beta_{ON}} \tag{3.13}$$

(b) In the 'off' region of the BJT-JFET, the BJT is in the saturation mode. Both the emitter-base junction and the collector-base junction are forward biased. The base current therefore has to support hole injection into the emitter and the collector as well as support recombination in the base.

For simplicity, it shall be assumed that the emitter and the collector are symmetrical, i.e., same dopant concentration and equally forward biased with respect to the base (Fig. 3.2(c)). It is then obvious from a comparison of Figs. 3.2(b) and 3.2(c) that
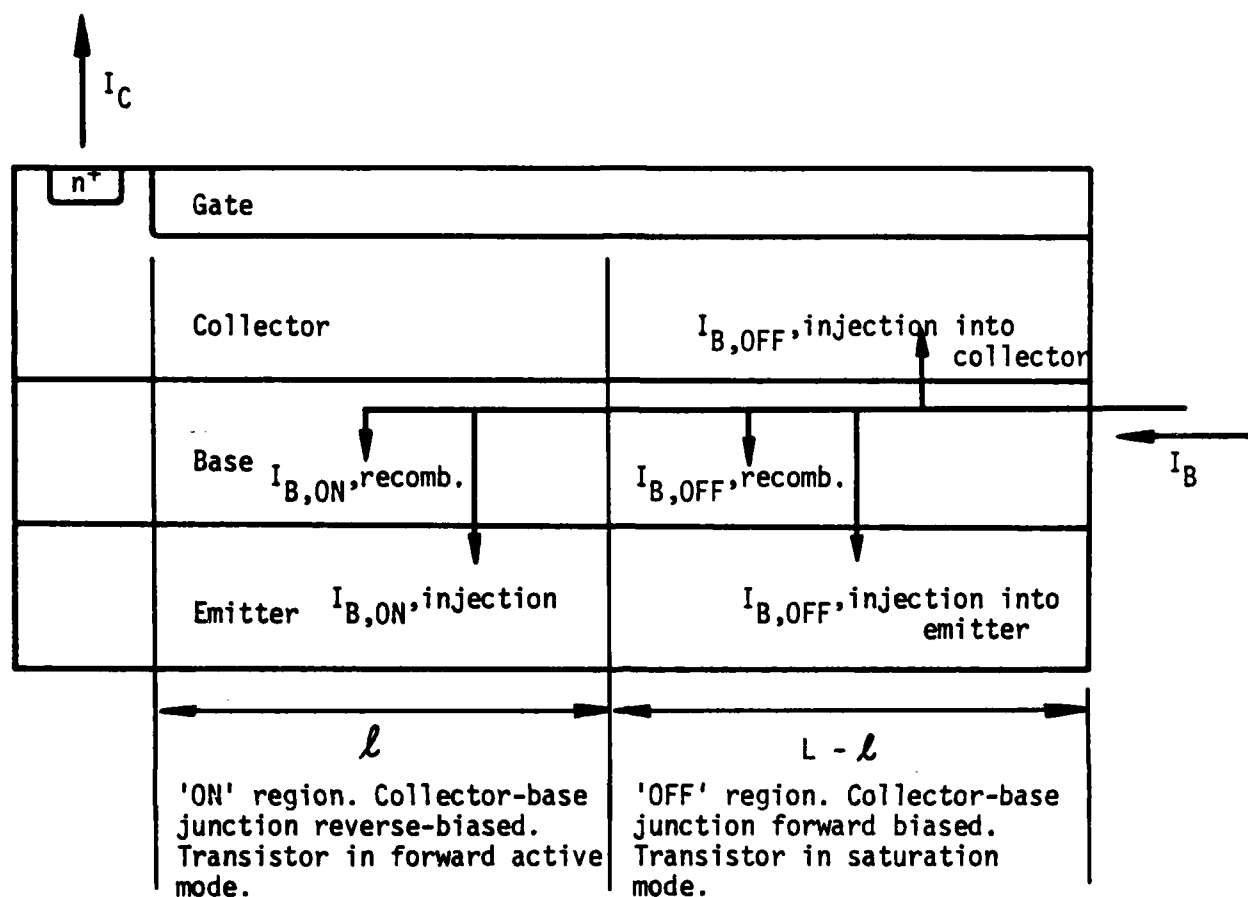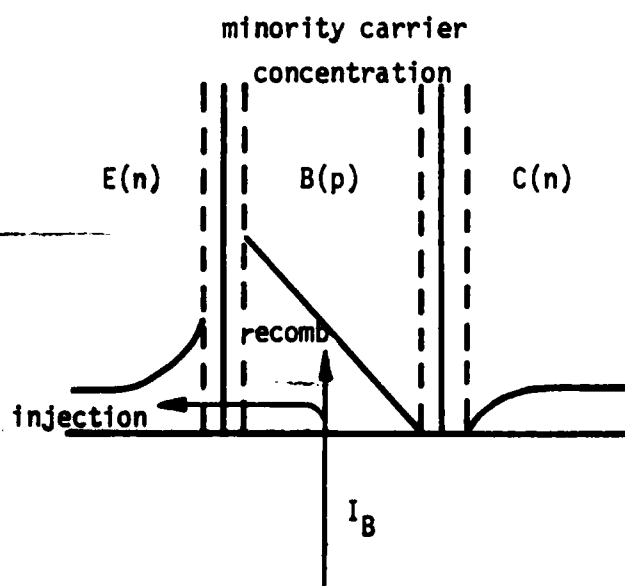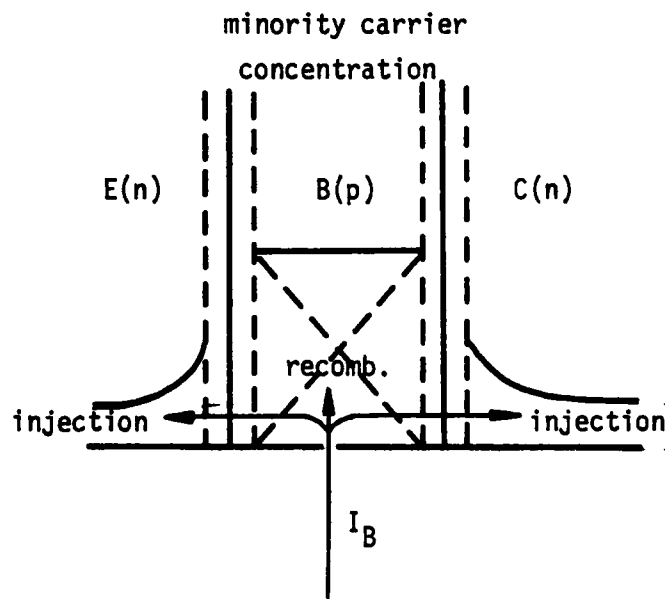
-20-

Fig. 3.2(a)

Fig. 3.2(b)

Fig. 3.2(c)

$$J_{B,OFF,recombination} = 2 \times J_{B,ON,recombination} \tag{3.14}$$

and

$$J_{B,OFF,injection} = 2 \times J_{B,ON,injection} \tag{3.15}$$

Therefore

$$J_{B,OFF} = 2 \times J_{B,ON} = \frac{2J_C}{\beta_{ON}} \tag{3.16}$$

The total base current of the BJT-JFET

$$I_B = I_{B,ON} + I_{B,OFF} \tag{3.17}$$

i.e.
$$I_B = J_{B,ON} W\ell + J_{B,OFF}W(L-\ell) \tag{3.18}$$

i.e.
$$I_B = \frac{J_C}{\beta_{ON}} W + \frac{2J_C}{\beta_{ON}} W(L-\ell) \tag{3.19}$$

i.e.
$$I_B = \frac{1}{\beta_{ON}} J_C W(2L-\ell) \tag{3.20}$$

Rearranging Eq. (3.20),

$$J_C = \frac{\beta_{ON}I_B}{W(2L-\ell)} \tag{3.21}$$

By substituting Eq. (3.21) into Eq. (3.12) a quadratic equation in ℓ is obtained:

$$\ell^2 + \left[\frac{2W}{\beta_{ON}I_B\rho} f(V_{DE},V_{GE})\right]\ell - \frac{4WL}{\beta_{ON}I_B\rho} f(V_{DE},V_{GE}) = 0 \tag{3.22}$$

where
$$f(V_{DE},V_{GE}) = V_{DE}t - \frac{2}{3}\left(\frac{2\varepsilon_s}{qN_d}\right)^{\frac{1}{2}}\left[(V_{bi}-V_{GE}+V_{DE})^{3/2} - (V_{bi}-V_{GE})^{3/2}\right]$$
$$- \frac{2}{3}\left(\frac{2\varepsilon_s}{qN_d}\right)^{\frac{1}{2}}\left[(V_{bi}-V_{BE}+V_{DE})^{3/2} - (V_{bi}-V_{BE})^{3/2}\right] \tag{3.23}$$

By writing

$$f_1(\beta_{ON},I_B,V_{DE},V_{GE}) = \frac{2W}{\beta_{ON}I_B\rho} f(V_{DE},V_{GE}) \tag{3.24}$$

Equation (3.22) can be rewritten as

$$\ell^2 + f_1(\beta_{ON},I_B,V_{DE},V_{GE})\ell - 2f_1(\beta_{ON},I_B,V_{DE},V_{GE})L = 0 \tag{3.25}$$

for which the solution is

$$\ell = \frac{1}{2}\left[-f_1 + (f_1^2 + 8f_1 L)^{\frac{1}{2}}\right] \tag{3.26}$$

the other (negative) root of the quadratic equation for ℓ being inadmissible.

ℓ is the effective channel length of the BJT-JFET, that is, the portion of the channel that constitutes the 'on' portion of the device. It is shown in Eq. (3.22) that ℓ is a function of I_B, V_{DE} and V_{GE}. Given the values of these variables and device parameters such as ρ, N_d, etc., the effective channel length ℓ can be determined.

Once the effective channel length ℓ of the BJT-JFET under a given set of bias conditions has been calculated, the collector/drain current I_C can be determined. The collector/drain current is the sum of the current injected into the channel/collector in the 'on' position of the device, that is

$$I_C = J_c W \ell \tag{3.27}$$

Upon substitution for J_c,

$$I_C = \beta_{ON} I_B \frac{W\ell}{W(2L-\ell)} \tag{3.28}$$

i.e.

$$I_C = \beta_{ON} I_B \frac{\ell}{2L-\ell} \tag{3.29}$$

Equation (3.29) expresses the collector/drain current I_C in terms of the base current I_B, the gain β_{ON} of the 'on' portion of the BJT-JFET, the overall length of the FET channel L and the effective channel length ℓ. If the entire channel is active, the effective channel length $\ell=L$, the physical channel length and Eq. (3.29) reduces to the familiar BJT equation

$$I_C = \beta_{ON} I_B \ , \tag{3.30}$$

as expected. If part of the channel is 'off', the BJT equation (3.30) is modified by the term $\ell/(2L-\ell)$. ℓ itself is a function of I_B, V_{DE} and V_{GE}, as expressed by Eqs. (3.22), (3.23), (3.24) and (3.25). Thus, Eqs. (3.26), (3.23), (3.24) and (3.29) together express IC as an implicit function of I_B, V_{DE} and V_{GE}. These equations are repeated here ease of reference:

$$I_C = \beta_{ON} I_B \frac{\ell}{2L-\ell} \tag{3.29}$$

$$\ell = \frac{1}{2}\left[-f_1 + (f_1^2 + 8f_1 L)^{\frac{1}{2}}\right] \tag{3.26}$$

$$f_1(\beta_{ON}, I_B, V_{DE}, V_{GE}) = \frac{2W}{\beta_{ON} I_B \rho} f(V_{DE}, V_{GE}) \tag{3.24}$$

$$f(V_{DE}, V_{GE}) = V_{DE}t - \frac{2}{3}\left(\frac{2\varepsilon_s}{qN_d}\right)^{\frac{1}{2}}\left[(V_{bi}-V_{GE}+V_{DE})^{3/2} - (V_{bi}-V_{GE})^{3/2}\right]$$

$$- \frac{2}{3}\left(\frac{2\varepsilon_s}{qN_d}\right)^{\frac{1}{2}}\left[(V_{bi}-V_{BE}+V_{DE})^{3/2} - (V_{bi}-V_{BE})^{3/2}\right] \tag{3.23}$$

The above Eqs. (3.29), (3.26), (3.24) and (3.23) can be simplified under certain conditions. In Eq. (3.23) the term

$$\frac{2}{3}\left(\frac{2\epsilon_s}{qN_d}\right)^{\frac{1}{2}}[(V_{bi}-V_{BE}+V_{DE})^{3/2} - (V_{bi}-V_{BE})^{3/2}]$$

represents the narrowing of the channel due to the depletion layer at the base/ channel junction while the term

$$\frac{2}{3}\left(\frac{2\epsilon_s}{qN_d}\right)^{\frac{1}{2}}[(V_{bi}-V_{GE}+V_{DE})^{3/2} - (V_{bi}-V_{GE})^{3/2}]$$

represents the narrowing of the channel due to the depletion layer at the gate/ channel junction. Since $V_{BE} = +0.7$ volt whereas V_{GE} can range from 0 volt to, say, -4 volts,

$$(V_{bi}-V_{BE}+V_{DE})^{3/2} \ll (V_{bi}-V_{GE}+V_{DE})^{3/2} \tag{3.31}$$

and to a first approximation, the modulation of the channel width by the base/ channel junction can be neglected and the corresponding term in Eq. (3.23) dropped.

Under certain circumstances another simplification to Eq. (3.23) can be made. Equation (3.23) is derived under the assumption that the JFET is operating under non-saturation conditions. When

$$V_{DE} = \frac{qN_d t^2}{2\epsilon_s} - (V_{bi}-V_{GE}) \tag{3.32}$$

the channel will pinch-off at the drain end and the collector/drain current I_C, for a given I_B and V_{GE}, saturates. Under such conditions, Eq. (3.23) can be further simplified to

$$f(V_{GE}) = \frac{1}{3}\frac{qN_d t^2}{2\epsilon_s} - (V_{bi}-V_{GE})\left[1 - \frac{2}{3}\left\{\frac{2\epsilon_s}{qN_d t^2}(V_{bi}-V_{GE})\right\}^{\frac{1}{2}}\right]. \tag{3.33}$$

Equation (3.33) can then be substituted into Eq. (3.24) for $f_1(I_B,V_{GE})$, which in turn can be substituted into Eq. (3.26) to determine the effective channel length ℓ of the BJT-JFET.

To illustrate the nonlinear properties of the BJT-JFET, two graphs have been plotted using the equations derived above. Figure 3.3 shows a plot of the normalized effective channel length $L_{eff}(=\ell/L)$ as a function of I_B and V_{GE} while Fig. 3.4 shows a plot of the drain current I_D versus I_B and V_{GE}. For both these plots, the following parameter values for the BJT-JFET are assumed:

Actual (physical) length of channel	$L = 0.2$ cm,
Width (lateral dimension) of device	$W = 0.2$ cm,
Width of channel (undepleted)	$t = 2$ μm,
Doping in the channel	$N_d = 10^{15}$ cm-3,
Resistivity of the channel	$\rho = 5$ ohm-cm,
Built-in potential across a p-n junction	$V_{bi} = 0.7$ volt.

NORMALIZED EFFECTIVE CHANNEL LENGTH Leff versus Ib AND Vge

$\beta = 50$
$V_{GE} = 0$

$\beta = 50$
$V_{GE} = -1$

$\beta = 50$
$V_{GE} = -2$

BASE CURRENT (MicroAmp)

Fig. 3.3

NORMALIZED EFFECTIVE CHANNEL LENGTH Leff
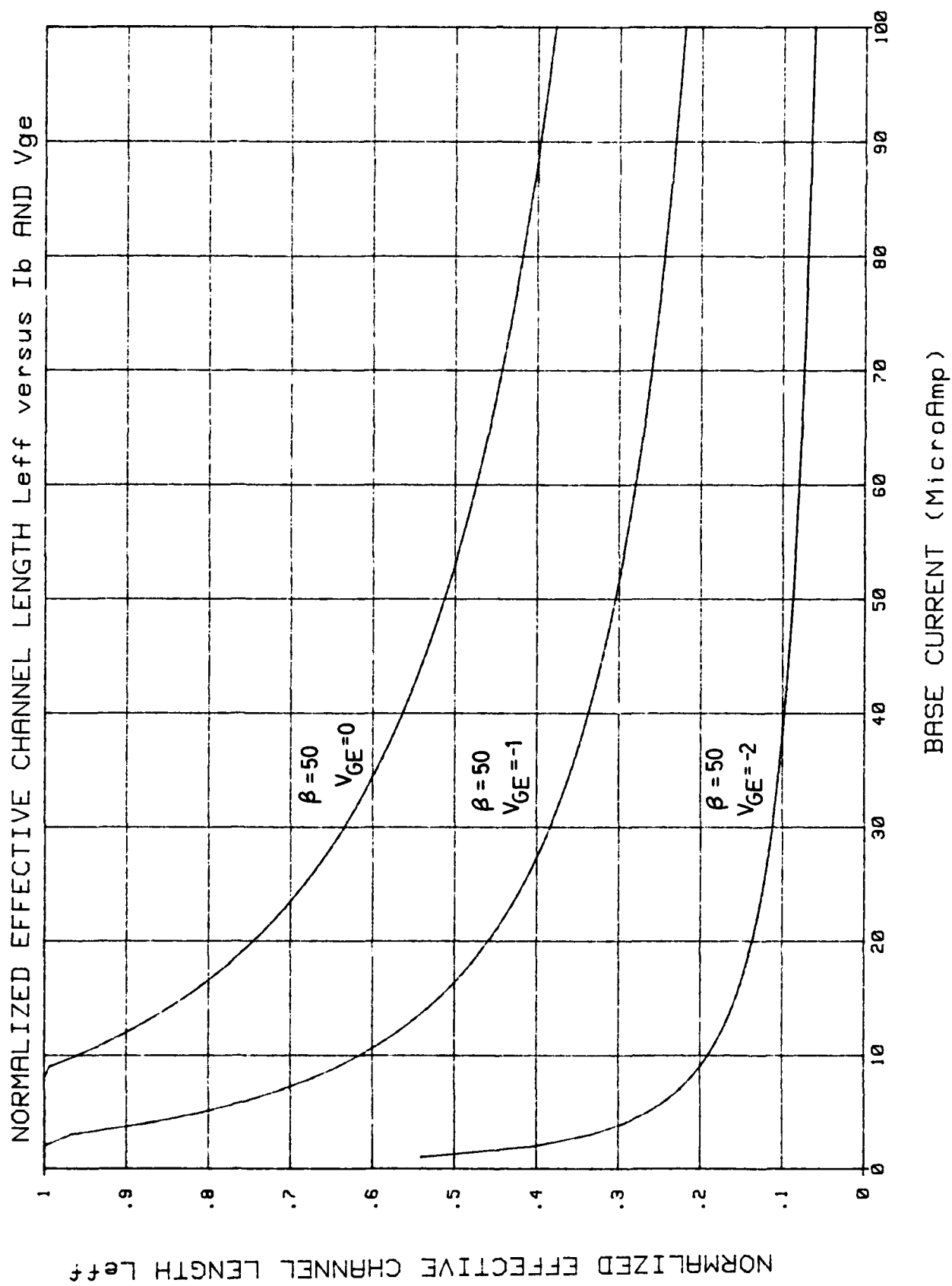
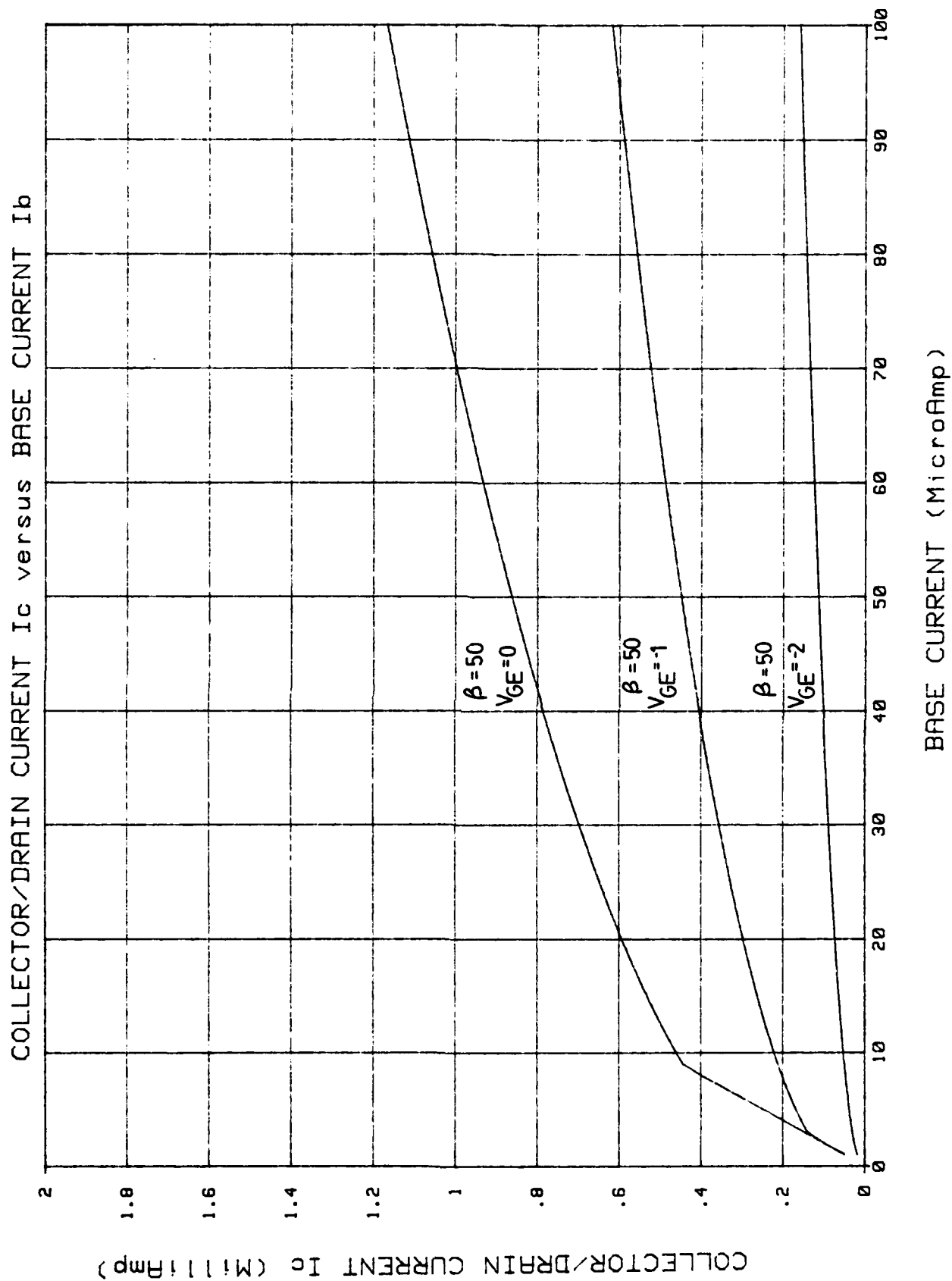COLLECTOR/DRAIN CURRENT Ic versus BASE CURRENT Ib

Fig. 3.4

The graphs are plotted for I_B ranging from 1 μA to 100 μA and V_{GE} from 0 volt to -2 volts. It is found that for low I_B, the effective channel length ℓ computed with Eqs. (3.26), (3.24) and (3.33) exceeds the actual channel length L. Since Eqs. (3.26), (3.24) and (3.33) are derived under the assumption that a portion of the BJT-JFET is 'off', the results for low I_B show that this assumption is not valid and that the entire BJT-JFET is in fact 'on'.* Under such conditions, ℓ is set equal to L, i.e., $L_{eff}=1$. As I_B increases, part of the BJT-JFET turns off and $L_{eff}<1$. The decrease in L_{eff} is more pronounced when there is a reverse bias on the gate. The nonlinearity produced by part of the channel turning 'off under high I_B and $|V_{GE}|$ also shows up in Fig. 3.4, in which I_C initially increases rapidly with I_B, but, as I_B increases, the rate of increase of I_C becomes less and less. These nonlinearities are useful in applications such as harmonic generation and the mixing of signals.

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*This result is consistent with the qualitative description of BJT-JFET operation discussed in Section (1).

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